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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/736,393	12/15/2003	William C. Moyer	SC13054TH	6215

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/736,393	MOYER ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 7-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-24* is/are allowed.

6)☒ Claim(s) *1-4,7 and 8* is/are rejected.

7)☒ Claim(s) *9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *19 October 2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-4 and 7-24 have been considered. Claims 5-6 have been cancelled as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 19 October 2005 and IDS as received on 19 October 2005.

Allowable Subject Matter

3. Claim 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. The following is a statement of reasons for the indication of allowable subject matter: Prior art searched did not teach or even suggest allocating a BTB entry based upon whether or not "the branch instruction was not loaded into a predetermined slot of a prefetch buffer and no other stall condition will occur" and whether or not "the branch target address can be obtained without causing a further stall condition in the pipelined data processing system". Prior art has taught and/or suggested allocating BTB entries based upon no other stall conditions occurring and has taught and/or suggested a prefetch buffer containing branch instructions. However, the prior art does not teach and/or suggest allocating a BTB entry based upon if a branch instruction is not loaded into a predetermined slot of a prefetch buffer and no other stall condition occurring.

5. Claims 10-24 are allowed.

6. The following is an examiner's statement of reasons for allowance: In regards to claims 10-15, prior art searched did not teach or even suggest allocating a BTB entry based upon whether or not "the branch instruction are not loaded into a predetermined slot of a prefetch buffer and no other stall condition will occur" and whether or not "the branch target address can be obtained without causing a further stall condition in the pipelined data processing system". In regards to claims 16-24, prior art searched did not teach or even suggest allocating a BTB entry if the branch instruction is not detected in a predetermined slot of the plurality of slots of the prefetch buffer." Prior art has taught and/or suggested allocating BTB entries based upon no other stall conditions occurring and has taught and/or suggested a prefetch buffer containing branch instructions. However, the prior art does not teach and/or suggest allocating a BTB entry based upon if a branch instruction is not loaded into a predetermined slot of a prefetch buffer.

7. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claim 1 is rejected under 35 U.S.C. 102(b) as being taught by Nakanishi, U.S. Patent Number 5,835,754 (herein referred to as Nakanishi). Nakanishi has taught a method for

allocating entries in a branch target buffer (BTB) in a pipelined data processing system, comprising:

a. Fetching instructions from a plurality of instructions (Nakanishi Abstract; column 1, lines 12-15; Figure 1; and Figure 2);

b. Determining that one of the plurality of instructions is a branch instruction (Nakanishi Abstract; column 1, lines 12-22; column 6, lines 13-19; column 8, lines 19-21 and 35-54; Figure 1; Figure 6; and Figure 7);

c. Decoding the branch instruction to determine a branch target address (Nakanishi Abstract; column 1, lines 12-22; column 6, lines 13-19; column 8, lines 19-21 and 35-54; Figure 1; Figure 6; and Figure 7);

d. Determining if the branch target address location can be obtained without causing a further stall condition in the pipelined data processing system (Nakanishi Abstract; column 1, lines 12-15; column 1, line 54 to column 2, line 7; column 2, lines 55-67; column 3, lines 29-33 and 48-55; column 6, lines 13-19; column 8, lines 19-21 and 35-54; column 10, lines 1-16; Figure 1; Figure 6; and Figure 7); and

e. Selectively allocating a BTB entry based on the determination (Nakanishi Abstract; column 1, lines 12-15; column 1, line 54 to column 2, line 7; column 2, lines 55-67; column 3, lines 29-33 and 48-55; column 6, lines 13-19; column 8, lines 19-21 and 35-54; column 10, lines 1-16; Figure 1; Figure 6; and Figure 7).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 2-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakanishi, U.S. Patent Number 5,835,754 (herein referred to as Nakanishi) in view of Rupley, II et al., U.S. Patent Number 6,057,998 (herein referred to as Rupley).

12. Referring to claims 2, 4, and 5, Nakanishi has not taught

a. Wherein determining if the branch target address location can be obtained further comprises examining a predetermined slot of a prefetch buffer having a plurality of slots to identify the branch instruction (Applicant's claim 2).

b. Wherein the predetermined slot of the prefetch buffer is characterized as being a first slot (Applicant's claim 4).

c. Wherein determining further comprises examining a predetermined slot of a prefetch buffer having a plurality of slots to identify the branch instruction (Applicant's claim 5).

13. Rupley has taught

a. Wherein determining if the branch target address location can be obtained further comprises examining a predetermined slot of a prefetch buffer having a plurality of slots to identify the branch instruction (Applicant's claim 2) (Rupley column 6, lines 19-36 and 41-45; column 6, line 56 to column 7, lines 1-14; and Figure 3).

b. Wherein the predetermined slot of the prefetch buffer is characterized as being a first slot (Applicant's claim 4) (Rupley column 6, lines 19-36 and 41-45; column 6, line 56 to column 7, lines 1-14; and Figure 3).

c. Wherein determining further comprises examining a predetermined slot of a prefetch buffer having a plurality of slots to identify the branch instruction (Applicant's claim 5) (Rupley column 6, lines 19-36 and 41-45; column 6, line 56 to column 7, lines 1-14; and Figure 3).

14. A person or ordinary skill in the art at the time the invention was made would have recognized, and as taught by Rupley, that examining a slot of a prefetch buffer to identify a branch instruction improves allocation of resources and performance (Rupley column 1, lines 55-63). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the determination of Rupley in the device of Nakanishi to improve resource allocation and performance.

15. Referring to claim 3, Nakanishi has taught loading a branch target address corresponding to the branch instruction into a predetermined entry of the BTB (Nakanishi Abstract; column 1, lines 12-15; column 1, line 54 to column 2, line 7; column 2, lines 55-67; column 3, lines 29-33 and 48-55; column 6, lines 13-19; column 8, lines 19-21 and 35-54; column 10, lines 1-16; Figure 1; Figure 6; and Figure 7).

16. Referring to claim 6, Nakanishi has taught using the branch target address in the BTB entry to prefetch a target instruction (Nakanishi Abstract; column 1, lines 12-15; column 1, line 54 to column 2, line 7; column 2, lines 55-67; column 3, lines 29-33 and 48-55; column 6, lines

13-19; column 8, lines 19-21 and 35-54; column 10, lines 1-16; Figure 1; Figure 6; and Figure 7).

17. Referring to claim 7, Nakanishi has taught

a. Determining that a stall condition exists in the data processing system (Nakanishi Abstract; column 1, lines 12-15; column 1, line 54 to column 2, line 7; column 2, lines 55-67; column 3, lines 29-33 and 48-55; column 6, lines 13-19; column 8, lines 19-21 and 35-54; column 10, lines 1-16; Figure 1; Figure 6; and Figure 7);

b. Determining that a BTB entry will not be allocated because of the stall condition (Nakanishi Abstract; column 1, lines 12-15; column 1, line 54 to column 2, line 7; column 2, lines 55-67; column 3, lines 29-33 and 48-55; column 6, lines 13-19; column 8, lines 19-21 and 35-54; column 10, lines 1-16; Figure 1; Figure 6; and Figure 7); and

c. Waiting for the branch instruction to be fetched from a memory location (Nakanishi Abstract; column 1, lines 12-15; column 1, line 54 to column 2, line 7; column 2, lines 55-67; column 3, lines 29-33 and 48-55; column 6, lines 13-19; column 8, lines 19-21 and 35-54; column 10, lines 1-16; Figure 1; Figure 6; and Figure 7).

18. Referring to claim 8, Nakanishi has taught using a first-in, first-out replacement algorithm to load the BTB (Nakanishi Abstract; column 1, lines 12-15; column 1, line 54 to column 2, line 7; column 2, lines 55-67; column 3, lines 29-33 and 48-55; column 6, lines 13-19; column 8, lines 19-21 and 35-54; column 10, lines 1-16; Figure 1; Figure 6; and Figure 7).

Response to Arguments

19. Applicant's arguments filed 19 October 2005 have been fully considered but they are not persuasive. Applicant argues in essence on pages 6-7

> Nakanishi does not determine if the branch target address location can be obtained without causing a further stall condition in the pipelined data processing system. Also, Nakanishi does not selectively allocate a BTB entry based on the determination.

20. This has not been found persuasive. Nakanishi in column 1, lines 23-29 describes that branch prediction is performed "simultaneously with instruction fetch, instead of waiting until whether the branch is taken or not is determined." This means that branch prediction prevents a stall condition from entering the pipeline, since it eliminates the wait that branch instructions would otherwise have created. Nakanishi also describes in column 1, lines 30-42 the effect of not having a correct branch prediction, e.g. a stall condition as well. Nakanishi then describes in column 1, line to column 2, line 7; column 6, lines 13-19; and column 8, lines 19-21 and 35-54 how the branch prediction mechanism accesses the branch target buffer for prediction information. When the branch prediction information is not contained in the buffer, meaning that an accurate prediction cannot be made, the processor either stalls, i.e. wait for the actual result, or just goes to the next sequential PC address, which is likely wrong since it is a random guess. Both situations cause stall conditions. Since the prediction information was not found in the buffer, Nakanishi describes in column 10, lines 1-16 allocating an entry in the buffer for the branch instruction based upon the current branch information to reduce the chances of the situations producing stall conditions from occurring again.

Conclusion

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

22. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

23. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
25 July 2005

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